## 10/600,065

## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application:

## Listing of Claims:

 (Currently Amended) An architecture that facilitates a reference voltage in a multi-bit memory, comprising:

a multi-bit memory core including a plurality of data cells for storing data;
first and second reference arrays of a plurality of multi-bit reference cells, the first and
second reference arrays fabricated on the memory core; and

a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage employed during a data cell read operation.

- 2. (Original) The architecture of claim 1, the core further comprising a sector of multi-bit data cells organized in rows and columns with associated wordlines (WLn) attached to the multi-bit data cells in a row and with associated bitlines (BLn) attached to the multi-bit data cells in a column, the first and second reference cells forming a multi-bit reference pair that is programmed and erased with the multi-bit data cells during programming and crase cycles.
- 3. (Original) The architecture of claim 2, the multi-bit reference pair is associated with a word in a wordline (WL0), the multi-bit reference pair utilized during reading of bits of the word.
- 4. (Original) The architecture of claim 2, the multi-bit reference pair is associated with multi-bit data cells in a wordline (WL0), the multi-bit reference pair utilized during reading of bits in the wordline (WL0).
- 5. (Original) The architecture of claim 2, further comprising a plurality of the multi-bit reference pairs associated with and attached to a corresponding wordline (WL0), the associated multi-bit reference pair utilized during reading of bits in the corresponding wordline (WL0).

- 6. (Original) The architecture of claim 2, the multi-bit reference pair is associated with multi-bit data cells in the sector, the multi-bit reference pair utilized during reading of bits in the sector.
- 7. (Original) The architecture of claim 1, the memory core including a plurality of data sectors that are accessible by the first and second reference arrays, the first and second reference arrays located centrally of the plurality of data sectors.
- 8. (Original) An integrated circuit comprising the memory of claim 1.
- 9. (Original) A computer comprising the memory of claim 1.
- 10. (Original) An electronic device comprising the memory of claim 1.
- 11. (Original) The architecture of claim 1, the first and second reference arrays including corresponding reference cells that are interweaved among the data cells.
- (Original) The architecture of claim 1, the memory core further comprising a plurality of data sectors, such that each data sector is associated with at least one of the first reference array and the second reference array of multi-bit reference cells.
- 13. (Currently Amended) An architecture that facilitates a reference voltage in a multi-bit memory, comprising:
- a multi-bit memory core for storing data, the memory core including two groups of data sectors;

first and second reference arrays of a plurality of multi-bit reference cells, the first and second reference arrays fabricated on the memory core interstitial to the groups of data sectors; and

a first bit value of a first reference cell of the first reference array and a second bit value of a second reference cell of the second reference array forming a reference pair whose respective bit values are averaged to arrive at the reference voltage for a read operation.

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- 14. (Original) The architecture of claim 13, the groups of data sectors read in an interleaved manner with a selected reference pair.
- 15. (Original) The architecture of claim 13, the first and second reference arrays precharged before being averaged.
- 16. (Original) The architecture of claim 13, further comprising a redundancy array located at least one of proximate and adjacent to the groups of data sectors.
- 17. (Currently Amended) A method for providing a reference voltage in a multi-bit memory, comprising:

receiving a multi-bit memory core for storing data;

providing first and second reference arrays of a plurality of multi-bit reference cells, the first and second reference arrays fabricated on the memory core; and

averaging a first bit value of a first reference cell of the first reference array with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage utilized during a read operation.

- 18. (Original) The method of claim 17, the core further comprising a sector of multi-bit data cells organized in rows and columns with associated wordlines (WLn) attached to the multi-bit data cells in a row and with associated bitlines (BLn) attached to the multi-bit data cells in a column, the first and second reference cells forming a multi-bit reference pair that is programmed and erased with the multi-bit data cells during programming and erase cycles.
- 19. (Original) The method of claim 18, the multi-bit reference pair is associated with a word in a wordline (WL0), the multi-bit reference pair utilized during reading of bits in the word.
- 20. (Original) The method of claim 18, the multi-bit reference pair is associated with multi-bit data cells in a wordline (WL0), the multi-bit reference pair utilized during reading of bits in the wordline (WL0).

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- 21. (Original) The method of claim 18, further comprising a plurality of the multi-bit reference pairs associated with and attached to a corresponding wordline (WL0), the associated multi-bit reference pair utilized during reading of bits in the corresponding wordline (WL0).
- 22. (Original) The method of claim 18, the multi-bit reference pair is associated with multi-bit data cells in the sector, the multi-bit reference pair utilized during reading of bits in the sector.
- 23. (Original) The method of claim 17, the memory core including a plurality of data sectors that are accessible by the first and second reference arrays, the first and second reference arrays located centrally of the plurality of data sectors.
- 24. (Currently Amended) A system for providing a reference voltage in a multi-bit memory, comprising:

means for providing a multi-bit memory core for storing data;

means for providing first and second reference arrays of a plurality of multi-bit reference cells, the first and second reference arrays fabricated on the memory core; and

means for averaging a first bit value of a first reference cell of the first reference array with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage to facilitate a read operation.

- 25. (Previously presented) The system of claim 24, the first and second reference arrays including corresponding reference cells that are interweaved among the data cells.
- 26. (Previously presented) The system of claim 24, the memory core further comprising a plurality of data sectors, such that each data sector is associated with at least one of the first reference array and the second reference array of multi-bit reference cells.
- 27. (Previously presented) The system of claim 24, further comprising a redundancy array located at least one of proximate and adjacent to the groups of data sectors.